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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2181	9

DATE MAILED: 10/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/825,818	VOGT ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed 4 April 2001 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Number 50 on Page 7 Line 24 and Page 8 Line 20. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Number 30 in Figure 4. A proposed drawing correction, corrected drawings, or

amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to because the bus grant signal is identified as GNT# on Page 7 Line 13, GNTx# in Figure 4, and GNTA# in Figure 5. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to because the TDI signal corresponding to Expansion Slot B 39 in Figure 5 is not connected to switches S4, S5, S6, and S7. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 2 and 3 recite the limitation "said hiding means" in Lines 1 and 2 of

Claim 2. There is insufficient antecedent basis for this limitation in the claim.

8. Claim 14 recites the limitation "said first peer device" in Line 3 of Claim 14. There is insufficient antecedent basis for this limitation in the claim.

9. Claim 14 recites the limitation "the second peer device" in Lines 2 and 3 of Claim 14. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1, 2, 4, 5, 6, 7, 8, 9, 15, 17, 18, 19, 20, 21, and 22 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Sacker et al. ("Sacker").

In reference to Claim 1, Sacker teaches a computer host coupled to first and second peer devices by a common bus (See Figures 1 and 2 and Column 2 Lines 24-

48) and a signal, generated when the first peer device is present, that hides the second peer device from the host (See Figure 2 and Column 3 Lines 26-32).

In reference to Claim 2, Sacker teaches the limitations as applied to Claim 1 above and further teaches the select signal supplied by the host to the second peer device being masked in the presence of the first peer device (See Figure 2 and Column 3 Lines 29-32).

In reference to Claim 4, Sacker teaches the limitations as applied to Claim 1 above and further teaches a Peripheral Component Interconnect (PCI) bus (See Column 2 Lines 30-35).

In reference to Claim 5, Sacker teaches the limitations as applied to Claim 4 above and further teaches that the host bus adapter (HBA), which comprises a processor, can enhance a SCSI device to allow it to perform RAID functions, and thus inherently functions as a RAID processor (See Figure 2 and Column 2 Lines 55-57).

In reference to Claim 6, Sacker teaches the limitations as applied to Claims 5 above and further teaches a Zero Channel RAID adapter. Since Zero Channel RAID requires an I/O controller provided in the motherboard of the circuitry to interface with the I/O device it is inherent that there is a motherboard mounted I/O controller working with the I/O device taught by Sacker (See Figure 2 and Column 1 Lines 31-43).

In reference to Claim 7, Sacker teaches the limitations as applied to Claim 6 above and further teaches that the I/O controller is mounted in the motherboard of the host (See Column 1 Lines 41-43).

In reference to Claim 8, Sacker teaches the limitations as applied to Claim 7 above and further teaches the RAID processor is located on an add-in card (See Figure 2 and Column 2 Lines 49-57).

In reference to Claim 9, Sacker teaches the limitations as applied to Claim 1 above and further teaches that the select signal from the host device is passed to the second peer device in the absence of the first peer device, since the absence of the card means the signal is not driven low and therefore does not turn off the switch (See Figure 2 and Column 3 Lines 26-32).

In reference to Claim 15, Sacker teaches a computer host coupled to first and second peer devices by a common bus (See Figures 1 and 2 and Column 2 Lines 24-48), a generating module configured to supply a signal indicating the presence of a first peer device (Figure 2 and Column 3 Lines 26-41), and a hiding module configured to hide a second peer device from the host so that the second peer device is controlled by the first peer device whenever the signal indicates the presence of the first peer device (See Figure 2 and Column 3 Lines 26-32).

In reference to Claim 17, Sacker teaches the limitations as applied to Claim 15 above and further teaches a PCI bus (See Column 2 Lines 30-35).

In reference to Claim 18, Sacker teaches the limitations as applied to Claim 17 above and further teaches that the HBA, which comprises a processor, can enhance a SCSI device to allow it to perform RAID functions, and thus inherently functions as a RAID processor (See Figure 2 and Column 2 Lines 55-57).

In reference to Claim 19, Sacker teaches the limitations as applied to Claim 18 above and further teaches a Zero Channel RAID adapter. Since Zero Channel RAID requires an I/O controller provided in the motherboard of the circuitry to interface with the I/O device it is inherent that there is a motherboard mounted I/O controller working with the I/O device taught by Sacker (See Figure 2 and Column 1 Lines 31-43).

In reference to Claim 20, Sacker teaches the limitations as applied to Claim 19 above and further teaches that the I/O controller is mounted in the motherboard of the host (See Column 1 Lines 41-43).

In reference to Claim 21, Sacker teaches the limitations as applied to Claim 20 above and further teaches the RAID processor is located on an add-in card (See Figure 2 and Column 2 Lines 49-57).

In reference to Claim 22, Sacker teaches the limitations as applied to Claim 15 above and further teaches that the select signal from the host device is passed to the second peer device in the absence of the first peer device, since the absence of the card means the signal is not driven low and therefore does not turn off the switch (See Figure 2 and Column 3 Lines 26-32).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 3, 10, 11, 12, 13, 14, 16, 24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sacker as applied to Claims 1, 2, 4, 5, 6, 7, 8, 9, and 15 above and further in view of DeWoskin.

In reference to Claim 3, Sacker teaches the limitations as applied to Claim 2 above (See Figures 1 and 2, Column 2 Lines 24-48, and Column 3 Lines 26-32). Sacker does not teach propagating a bus grant signal configured to grant exclusive control rights of the second peer device to the first peer device. DeWoskin teaches a grant signal used to grant exclusive access of a bus to a controller to access a memory interface (See Abstract and Column 1 Lines 32-56 of DeWoskin).

In reference to Claim 10, Sacker teaches providing one or more expansion slots configured to receive a respective add-in card including a processor thereon (See Figure 2 and Column 2 Lines 49-57 of Sacker), generating a signal indicative of the presence of said add-in card in one of the expansion slots (See Figure 2 and Column 3 Lines 26-32), and masking a host device select signal generally used by said host to assert control of a controller on the motherboard of said host in response to said signal indicative of the presence of said add-in card (See Figure 2, Column 1 Lines 31-43 and Column 3 Lines 29-32). Sacker does not teach propagating a bus grant signal configured to grant control rights to the processor on said add-in card, in lieu of said host, over said controller. DeWoskin teaches a grant signal used to grant control rights

to a controller (analogous to the processor of Claim 10) to access a memory interface (analogous to the controller of Claim 10) (See Abstract and Column 1 Lines 32-56 of DeWoskin).

In reference to Claim 11, Sacker teaches the limitations as applied to Claim 10 above, and further teaches a PCI bus (See Column 2 Lines 30-35 of Sacker). Sacker does not teach propagating a bus grant signal configured to grant control rights to the processor on said add-in card, in lieu of said host, over said controller. DeWoskin teaches a grant signal used to grant control rights to a controller (analogous to the processor of Claim 10) to access a memory interface (analogous to the controller of Claim 10) (See Abstract and Column 1 Lines 32-56 of DeWoskin).

In reference to Claim 12, Sacker teaches the limitations as applied to Claim 11 above and further teaches the RAID processor is located on an add-in card (See Figure 2 and Column 2 Lines 49-57 of Sacker). Sacker does not teach propagating a bus grant signal configured to grant control rights to the processor on said add-in card, in lieu of said host, over said controller. DeWoskin teaches a grant signal used to grant control rights to a controller (analogous to the processor of Claim 10) to access a memory interface (analogous to the controller of Claim 10) (See Abstract and Column 1 Lines 32-56 of DeWoskin).

In reference to Claim 13, Sacker teaches the limitations as applied to Claim 12 above and further teaches the controller on the motherboard of the host comprising an I/O controller (See Column 1 Lines 41-43 of Sacker). Sacker does not teach propagating a bus grant signal configured to grant control rights to the processor on

said add-in card, in lieu of said host, over said controller. DeWoskin teaches a grant signal used to grant control rights to a controller (analogous to the processor of Claim 10) to access a memory interface (analogous to the controller of Claim 10) (See Abstract and Column 1 Lines 32-56 of DeWoskin).

In reference to Claim 14, Sacker teaches the limitations as applied to Claim 10 above and further teaches the select signal supplied by the host to the second peer device being masked in the presence of the first peer device (See Figure 2 and Column 3 Lines 29-32 of Sacker). Sacker does not teach propagating a bus grant signal configured to grant control rights to the processor on said add-in card, in lieu of said host, over said controller. DeWoskin teaches a grant signal used to grant control rights to a controller (analogous to the processor of Claim 10) to access a memory interface (analogous to the controller of Claim 10) (See Abstract and Column 1 Lines 32-56 of DeWoskin).

In reference to Claim 16, Sacker teaches the limitations as applied to Claim 15 above, and further teaches a masking module configured to supply a signal indicative of the presence of a first peer device (See Figure 2 and Column 3 Lines 26-41 of Sacker). Sacker does not teach a propagating module configured to propagate a bus grant signal wherein said bus grant signal is configured to grant control rights to said first peer device over said second peer device. DeWoskin teaches a bus arbitrator that propagates a grant signal through a wire (analogous to the propagating module of Claim 16) to grant exclusive access of a bus to a controller (analogous to the first peer device

of Claim 16) to access a memory interface (analogous to the second peer device of Claim 16) (See Abstract and Column 1 Lines 32-56 of DeWoskin).

In reference to Claim 24, Sacker teaches the limitations as applied to Claim 16 above, and further teaches that the masking module is comprised of a plurality of switches. The masking module analogous circuitry of Sacker comprises two inverter logic gates and a transistor switch (See Figure 2 of Sacker). Since each inverter logic gate is inherently comprised of at least one switching device, said circuitry comprises a plurality of switching devices, as in Claim 24. Sacker does not teach a propagating module configured to propagate a bus grant signal wherein said bus grant signal is configured to grant control rights to said first peer device over said second peer device. DeWoskin teaches a bus arbitrator that propagates a grant signal through a wire (analogous to the propagating module of Claim 16) to grant exclusive access of a bus to a controller (analogous to the first peer device of Claim 16) to access a memory interface (analogous to the second peer device of Claim 16) (See Abstract and Column 1 Lines 32-56 of DeWoskin).

In reference to Claim 25, Sacker teaches the limitations as applied to Claim 16 above, and further teaches that the masking module is comprised of a plurality of logic gates. The masking module analogous circuitry of Sacker comprises two inverter logic gates and a transistor switch (See Figure 2 of Sacker). Sacker does not teach a propagating module configured to propagate a bus grant signal wherein said bus grant signal is configured to grant control rights to said first peer device over said second peer device. DeWoskin teaches a bus arbitrator that propagates a grant signal through a

wire (analogous to the propagating module of Claim 16) to grant exclusive access of a bus to a controller (analogous to the first peer device of Claim 16) to access a memory interface (analogous to the second peer device of Claim 16) (See Abstract and Column 1 Lines 32-56 of DeWoskin).

One of ordinary skill in the art at the time the invention was made would combine the device of Sacker with the arbitrator of DeWoskin, resulting in the inventions of Claims 3, 10, 11, 12, 13, 14, 16, 24, and 25, in order to prevent both bus masters (analogous to the host controller and first peer device) from simultaneously taking control of the second peer device (See Column 1 Lines 20-23 of DeWoskin).

14. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sacker and DeWoskin as applied to Claim 16 above, and further in view of Ganesan.

In reference to Claim 23, Sacker and DeWoskin teach the limitations as applied to Claim 16 above. Sacker and DeWoskin do not teach the propagating module comprising a flip-flop. Ganesan teaches the use of a flip-flop (See Abstract, Figures 1-3, and Column 1 Lines 1-23 of Ganesan).

One of ordinary skill in the art at the time the invention was made would combine the device of Sacker and DeWoskin with the flip-flop of Ganesan, resulting in the invention of Claim 23, in order to ensure that the bus grant signal is properly propagated to the second peer device regardless of noise that may occur on the line (See Column 1 Lines 13-17 of Ganesan).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The examiner can normally be reached on Monday-Thursday (8-5:30), Alt. Fridays (8-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-5631.

tjc